AN ADVANCED PACKAGING TECHNOLOGY FOR HIGH PERFORMANCE POWER DEVICES

Burhan Ozmat and Victor Temple
Harris Semiconductor
Latham New York 12110
Phone: (518) 782-1182, Fax: (518) 782 1185-1185

ABSTRACT

The emerging advanced power device technologies such as Mos Controlled Thyristor (MCT) and (IGBT) are pushing the current densities, switching speeds and frequencies to new dimensions. To fully utilize the capabilities of such devices there is a need to provide the electrical, structural and thermal environments compatible with their packaging requirements In response to these needs, HPR&D Center developed the Thin Pak (TP) technology and an integral compact heat exchanger technology both of which offer a new approach for the packaging of high performance power devices designed for commercial and military applications. The TP consists of a power device and a dielectric interposer or simply a lid, with a specific through hole pattern. Both surfaces and through holes of the lid are metalized to conduct current. The integral heat exchanger technology reduces the junction to ambient thermal resistance Rja to less than 0.04 ^{o}C/W for a module with a compact base area of 3 in^2. The low thermal resistance is due to eliminating the resistive interfaces, providing a large surface area and improved film coefficient. Some of the thermal structural and electrical aspects of these two emerging technologies will be reviewed, and experimental and modeling results will be presented.

INTRODUCTION

Performance, cost and the reliability of advanced dual use high performance discrete Semiconductor devices, and Power Modules are strongly impacted by the characteristics of their package. Thin Pack (TP), addresses these issues and offers one of the highest area (>90%) and volume efficient packaging technology for military and commercial applications of discrete Semiconductor power devices today. In the most general configuration, the TP package contains a combination of single or multiple discrete power devices and diodes (Figure 1).

TP has applications as a stand alone package and as a building block for power modules. For example, TPs of MOS Controlled Thyristor (MCT) type devices (Temple, 1984, Hingorani, 1993) with excellent surge current capabilities (Temple, 1993) have applications in power circuits for detonators and welding equipment. Power modules built with TP packages have a broad range of military and/or commercial applications in a wide range of power levels (Ozmat , 1997)

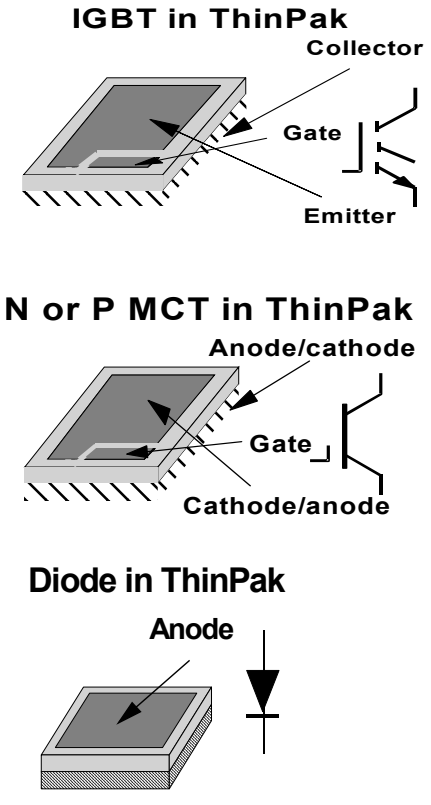

Figure 1. ThinPak packages reduce inductance and increase current capability. Package resistance and inductance are approximately 50 $\mu\Omega$, and 0.5 nH, respectively.

AN OVERVIEW OF TP

The key element of TP is a dielectric lid that contains patterns of metalization on the top and the bottom surfaces. The metalization pattern on the bottom surface of the lid matches that of the power device being MCT, IGBT or MOSFET or simply a diode so that the lid can be bonded to these devices. The standardization of die and lid metalization pattern allows the use of a single lid design for a family of power devices of a given size.

To complete a power circuit the top side of the lid is bonded to gate and gate return terminals, and to an anode terminal which is generally sheet metal with high electrical conductivity. TP can then be attached, similar to chip on board configuration, with conductive traces striplined with the anode. A pattern of metalized through holes provides the electrical conductivity through the lid and to the through thickness thermal conductivity of the lid. The matched metalization of the die and the lid over the gate and anode areas, when solder bonded, can offer an extremely low profile (~ 0.050" thick), surface mountable and low cost packages

Solder bonded ceramic lid and die approach eliminates the need for traditional wire bonding used to make contacts to power busses. The parasitic package inductance, resistivity, and reliability improves significantly. The extremely low inductance of the TP package (~ 0.5 nH) makes it ideally suitable for pulsed power and high surge current applications. The inherently low forward drop of MCT devices (< 1.5 V at ≥ 100 Amp/cm^2) when combined with the low resistance of HTP lid offers a high efficiency package with low power dissipation levels up to several tens of kHz switching frequencies. In addition, potential reliability problems associated with the thermal and vibrational fatigue of bond wires and fracturing of brittle semiconductor dies under the stress of multiple wire bonding processes are practically eliminated with this packaging approach.

The TP lid is fabricated in an array of multiple units. Various types of electronic grade ceramic materials, such as Al_2O_3, BeO and AlN, are available in sintered sheet forms suitable for lapping, laser machining and scribing to produce (nxm) lid arrays. Scribing and machining in the sintered form is required to meet the dimensional tolerance requirements for the lid metalizations (Figure 2).

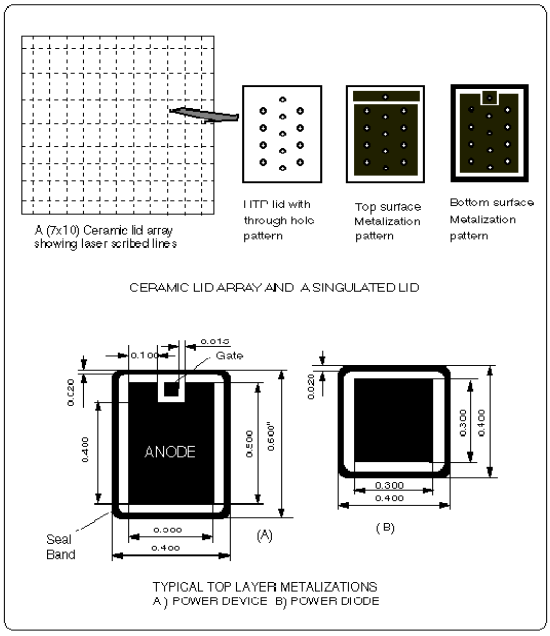

Figure 2. A Sketch of a ceramic lid array, a single lid with through holes and die and lid metalization.

Alternatively, the lid array may be fabricated from a high temperature organic laminate with laminated Cu layers by using the standard, double sided printed wire board technology. A laminate would be drilled and plated for metalized through holes and patterned for top and bottom metalizations. The lids would be singulated from the large laminate by, forexampe, stamping process for assembly. However, the moisture absorbtion, Cu thickness, CTE mismatch to silicon die, and maximum soldering temperature would be limited by the organic laminate material.

LID DESIGN AND METALIZATION

The lid design and its metalization deserves special attention. The most important functional and reliability requirements of the lid design and its metalization are: metal thickness, electrical resistance, inductance cost, ability to cover through holes of 2:1 aspect ratio or higher, and toughness and strength of metal to ceramic bond interfaces.

The top layer metalization of a power device

usually contains a combination of sputtered Ti, Al, Ni, Au based thin films with combined thickness of a couple of microns. This multilayer thin film metalization is not capable of carrying high current levels in its plane. In addition, the structural integrity, cost and soldering process requirements of the ceramic lid limit the number and the size of the electrical vias. Therefore, the in-plane resistance combined with the current crowding effect becomes an important factor that needs to be addressed by the lid design. The number and the size of holes as well as the metalization thickness will effect the inductance and the resistance of lid.

A typical high performance MCT type power die of 0.400"x0.600" dimensions with ≥ 200 Amp/cm^2 current capability contains more than a couple of hundreds of thousands cells with 20 micron ground rules. These current cells are paralleled to attain high current rating for the device. Successful parallel operation of these cells requires that a uniform electric potential be applied across the die surface. Otherwise puncturing of cells and shorting of the device becomes inevitable. Therefore, the number and the size of via holes and the thickness of lid metalization and the solder joint must be carefully selected.

Closed form solutions were developed to study the metalization, process and design requirements for HTP lids in a one dimensional model. Figure 3. shows an axisymmetric model of a via cell structure. To obtain a closed form solution for the potential drop across a via cell over the power die, the current flow was assumed to be radial in the anode power lead, in the solder joint and in the lid metalization. It was also assumed that the current is axial in the thin walled cylinder of via metalization and in the plug of solder.

The total resistance R_t of the current path from the power device to the edge of the Cu electrode can be viewed as three resistances in series.

R_{dv}:Resistance from die surface to via entry

R_V : Resistance of via (solder and lid metalization)

R_{VS}:Resistance from via exit to edge of Cu strap

$R_t=R_{dv}+R_V+R_{VS}$, where R_{dv} the resistance from die to via entrance is given by,

$$R_{dv}=\frac{\rho_m.\rho_s.J_o}{2.(\rho_m.t_s+\rho_s.t_m).I_c}\left[r_o^2.\ln\left(\frac{r_o}{r_i}\right)-\frac{1}{2}.(r_0^2-r_i^2)\right] \quad (1.1)$$

where

ρ_m = Specific resistance of lid material $(\mu\Omega-in)$
ρ_s = Specific resistance of solder $(\mu\Omega-in)$
J_o = Current density (A/in^2)
I_c = Current per via cell (Amp)
t_m = Thickness of lid metalization (in)
t_s = Thickness of solder (in)
r_i = Radius of via (in)
r_o = Radius of via cell (in)

The active die area (A_d) and number of vias per lid (n) defines the effective area (A_c) and the radius of the via cell and the cell current (I_c)

$$A_c=\left(\frac{A_d}{n}\right) \;;\; R_o=\sqrt{\frac{A_c}{\pi}} \;;\; I_c=J_o.A_c \qquad (1.2)$$

Resistance of the via (R_V) may be modeled as the resistances due to solder (R_S) and lid metalization (R_m) in parallel.

$$R_s=\frac{\rho_s.h}{\pi(r_i-t_m)^2} \;;\; R_m=\frac{\rho_m h}{\pi\left[r_i^2-(r_i-t_m)^2\right]} \qquad (1.3)$$

where (h) is the thickness of ceramic lid.

The resistance of the current path from the exit point of the via to the edge of the Cu strap (R_{VS}) is given by (1.4).

$$R_{vs}=\frac{\rho_c}{2\pi t_c}\ln\left(\frac{r_o}{r_i}\right) \qquad (1.4)$$

where:

ρ_c = specific resistance of Cu strap $(\mu\Omega-in)$
t_c = thickness of Cu strap (in)

The results of this analysis may be used to predict the dependence of the voltage drop across a via cell to the thickness of the lid metal (Al) and the thickness of the solder joint between the lid and the die. Figures 4 and 5 show such plots for two different values of via hole diameters, 0.040" and 0.020".

The following numerical values of parameters were used in the calculations:

$n = 12,\ h = 0.025\,in,\ A_d = 0.147\,in^2$
$J_o = 0.3x10^3\,A/in^2,\ t_c = 0.020\,in$
$\rho_s = 8.2\,\mu\Omega - in,\ \rho_m = 0.78\,\mu\Omega - in$
$\rho_C = 0.47\,\mu\Omega - in$

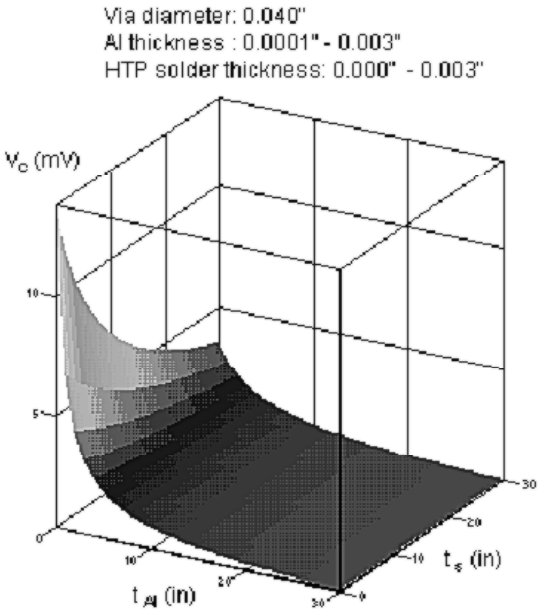

Figure 3. Effect of solder and lid metalization on the Voltage drop across a via cell with 0.020" diameter

The results of the analysis show that the performance and the reliable operation of TP strongly depend on the thickness of the lid metal. The solution predicts that the voltage drop across the power devices becomes singular as the metal and solder joint thickness approaches zero. However, the voltage drop becomes insensitive to both variables when the thickness of lid metalization exceeds 0.002". Experimental and device level modeling efforts have shown that the maximum voltage drop across the active surface of a size eight (0.600"x0.400") MCT device needs to be kept below 5 mV for essentially a uniform current flow. Therefore, the thickness of Al metalization needs to be specified as ≥ 0.002 inch to meet this requirement.

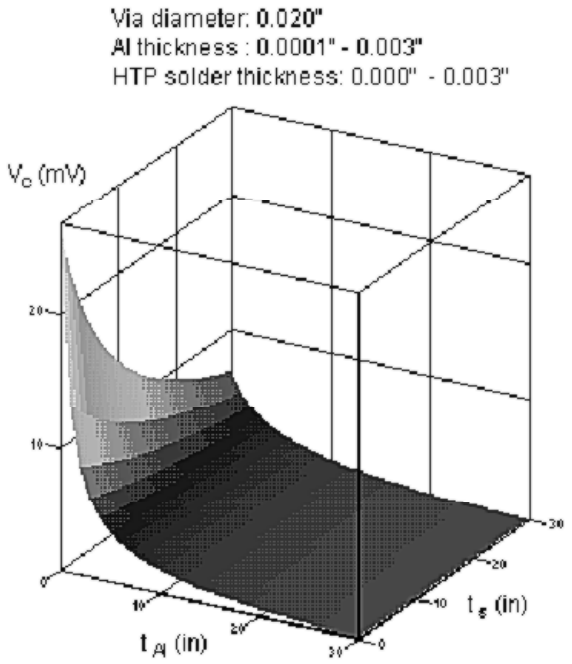

Figure 4. Effect of solder and lid metalization on the Voltage drop across a via cell with 0.040" diameter

The results also show that the voltage drop across the die surface is a sensitive function of the via diameter. Increasing the via diameter from 0.020" to 0.040" reduces the voltage drop by one half. However, solder bonding experiments show that as the via diameter increases, the control of solder joint thickness, uniform solder coverage at the die to lid interface, and forming the gate contact becomes difficult. The difficulty stems from the fact that the molten solder can easily leave the interface by flowing up through the via holes. Therefore, to eliminate assembly problems the via diameter should be kept about 0.020"

The accuracy of closed form solution was verified by using 2D FEM technique. The predictions of the closed form solution and the FEA are within 15% of each other (Ozmat, 1997).

The electrical performance of TP was verified by modeling and testing the inductance and resistance characteristics of metalized lid. The electrical model of metalized lid is shown in Figure 5. The model included top and bottom electrodes as 0.010" thick Cu copper straps bonded to TP and the device with 0.002" thick solder layers. The current distribution was assumed to be uniform in the Cu straps. The results of the electromagnetic field analysis showed that the current is pulled out from

each via uniformly and distributed on the bottom metalization of lid. The electromagnetic analysis of lid showed that the lid resistance and inductance are approximately 50 $\mu\Omega$ below 500kHz and 1nH when the power electrodes are striplined, respectively.

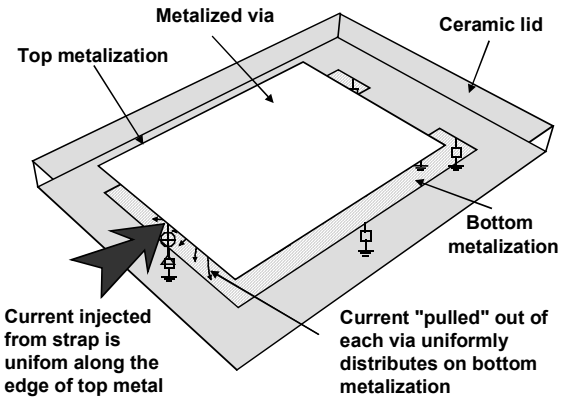

Figure 5. The electrical model of the lid geometry. Courtesy of PEBB-VTB Team, USC.

Experimentally, the lid inductance was estimated by using the test setup that the equivalent circuit diagram and the photographs of which are shown below. The lightly damped test circuit consisted of striplined power electrodes, a 5 $m\Omega$ low inductance CVR resistor, a 0.2 μF high voltage capacitor having low inductance and low ESR. The circuit inductance and capacitance was 0.2 μF and 3.6 nH without the TP switch, respectively.

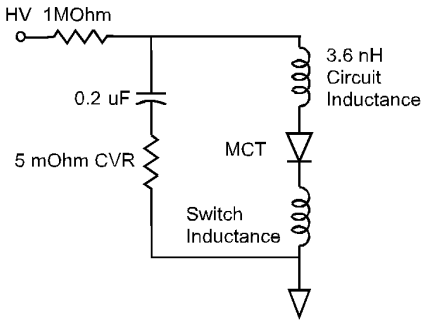

Figure 6 equivalent circuit diagram of the test set up for inductance measurements.

The high voltage capacitor was discharged either by mechanically shorting the power electrodes without TP or by switching the size 8 NMCT. The ringing waveform of the lightly damped RLC circuit was monitored and recorded through an oscilloscope Figure 8. The period of oscillations was compared for two cases and the lid inductance was back calculated from the increase in the period. The lid inductance value is 1nH 0.25nH when the power electrode are perpendicular and 0.5nH 0.25nH when striplined.

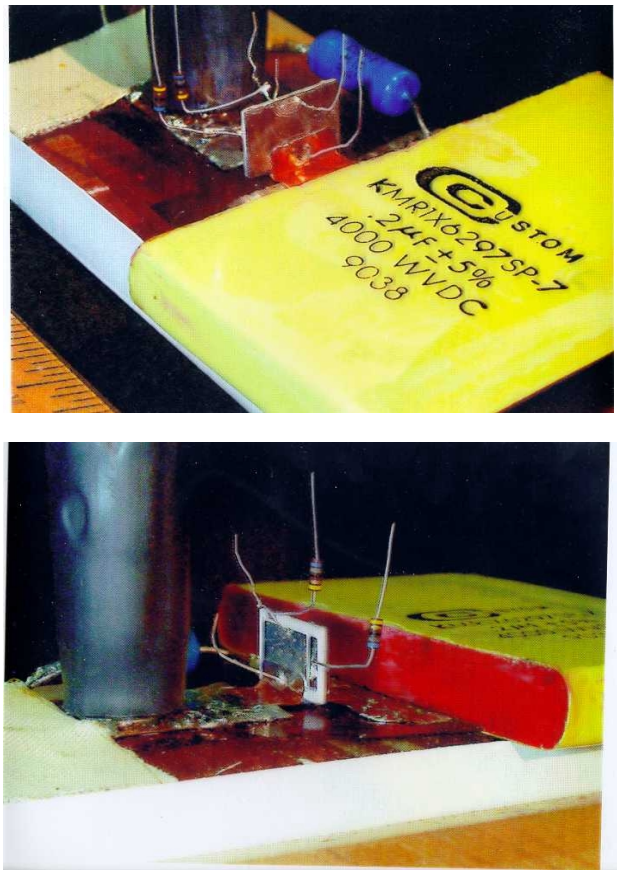

Figure 7. Pictures of the test set up for induction measurements, courtesy of Dr. Kwong Chu, Sandia Laboratories.

METALIZING HTP LID ARRAYS

To meet the metalization requirements for HTP lids, a cost effective and reliable approach was implemented. The new metalization technique applies 0.002" to 0.003" thick 1100 series Al metalization on both sides and through holes of lid arrays simultaneously in a single step at a rate of > 25 ^{o}A /second (Muehlberger, 1983). To provide and preserve a solderable metalization for the lid arrays, the blanket Al metalization layer is patterned

by a double sided unisotropic spray etch process through a toughened dry film photo resist. Patterned Al metalization then plated with an approximately 200 microinch thick Ni layer in a

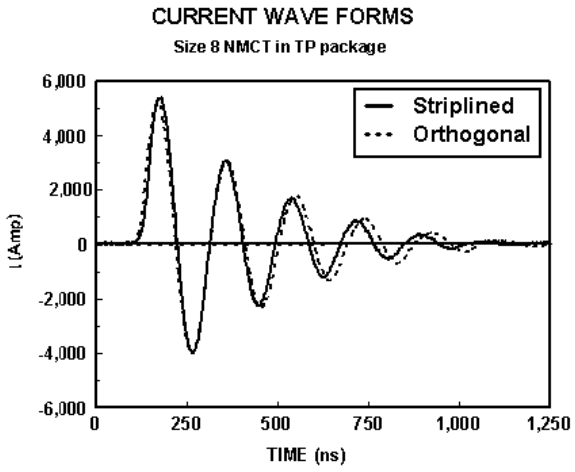

Figure 8. Current wave forms of the test circuit showing the effect of switch inductance

low phosphorus electroless solution. TP lid arrays are then plated with an approximately 10 microinch Au in an electroless or immersion Au bath. This last step is necessary to prevent the oxidation of Ni layer and thereby to preserve the solderability of TP lid metalization (Parquet, 1996, Stafstorm, 1997). The Figure 9 shows the processing steps for metalized TP lid arrays.

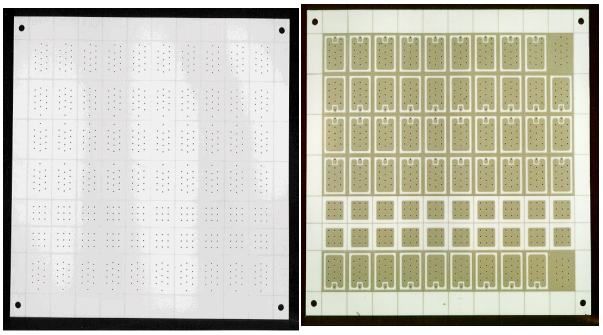

Figure 9. TP lid arrays, bare Al_2O_3 ceramic (left), after metalization, patterning and plating (right)

The Sabestian pull tests technique was routinely employed to evaluate the reliability of patterned and plated lid array metalization quantitatively. The technique requires that an Al pin is attached to the lid metalization by curing a specially developed epoxy resin that minimize the residual cure stresses at the metal-epoxy interfaces. The strength of the pre-coated epoxy is approximately ~14 Kpsi. Therefore, the epoxy-bonded pin may be used to test the adhesion strength up to 14 Kpsi. For measuring higher strength levels soldered or brazed pins are usually employed. Figure 10 shows a typical metalized lid before and after the sabestian pull test. As shown in the figure the adhesion strength of the patterned and plated Al metalization is usually higher that the strength of the base ceramic substrate resulting in ceramic pull outs > 8 Kpsi failure stress

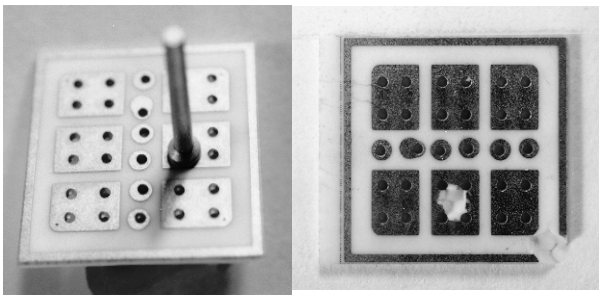

Figure 10 TP lids before and after sabestian pull test

The assembly process for a hermetic HTP package requires screening and reflowing power die and the lid separately. The screening uses a high lead content Pb/Sn type solder paste. Although the paste contains flux, the separately reflown parts could be thoroughly flux cleaned prior to final assembly. The final joining process is truly fluxless and it takes place in a reducing atmosphere. Figure 10 shows the various stages of an assembly process. for a hermetic HTP. The top row shows the singulated lids and power dies to be joined. The middle row shows the individually reflown and flux cleaned lids and power dies. The bottom row shows a hermetic HTP after the final fluxless joining process.

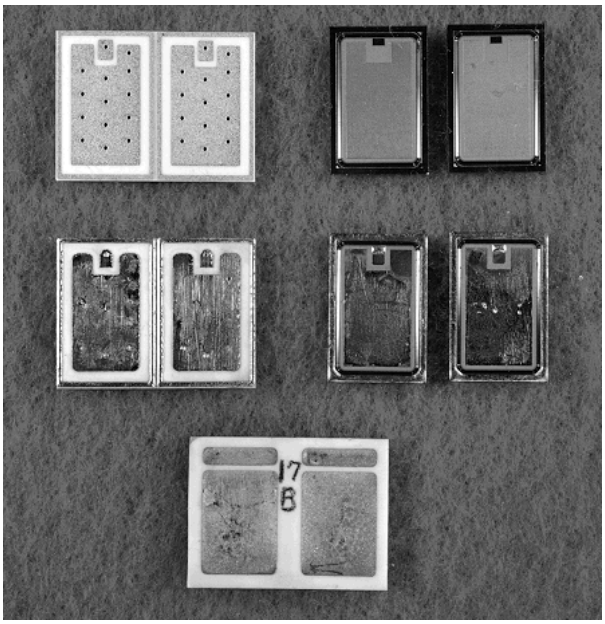

Figure 11. TP assembly process steps

THERMAL MANAGEMENT

Power modules integrate single switch or multiple switch configurations where in each switch multiple devices may be paralleled to offer improved current capacity, and/or functionality and performance. Therefore, a power module may function as a high capacity single switch, a Half Bridge or a Full Bridge.

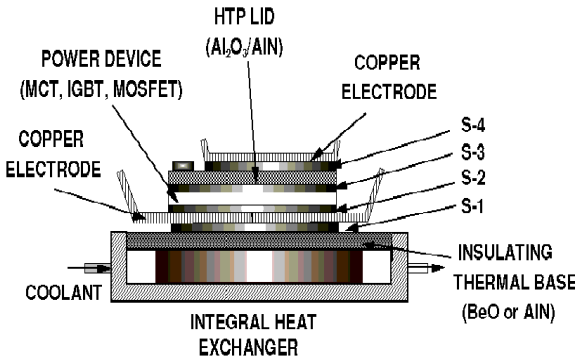

Figure 12. Cross-section of an advanced power module.

Internally, a typical power module consists of multiple layers of various materials such as ceramics, silicon, various solders of different compositions, metals polymers. Figure 12 shows a cross section of an advanced power module. Where S1. S2, S3 and S4 are the layers of various solders. TPs, electrodes and insulating thermal base are bonded with a combination of high melting point (s3) and low melting point Pb/Sn based solders compatible with the hierarchy of soldering processes.

Advanced power modules will be required to handle extremely high heat fluxes approaching 500 W/cm^2 at device level. For example, a typical MCT device with 1 cm^2 active area may conduct 250 Amp steady current through a 2 V forward drop, thereby dissipating 500W. A power module with 1000 Amp steady current rating may dissipate 2 KW in a non-switching application. For switching applications, the power dissipation levels will be higher. The combined effect of device characteristics, inductive loads and or parasitic package inductance will further increase the dissipation levels. Under such high dissipation levels the end users may have to significantly reduce the rating of power modules due to the limited heat sinking capability. To address this concern advanced power module designs may incorporate high performance integral heat exchangers. Such an approach may improve the rating of power modules and take better advantage of the capabilities of the advanced power devices. From the end user point of view it is a more complete solution and allows the customer to focus on the application itself rather than dealing with heat sinking.

The integral compact heat exchanger eliminates the highly resistive external thermal interfaces such as thermal pads, thermal pastes or thermal epoxies used to couple the power modules with external air cooled or liquid cooled heat sinks (Sorgo, 1996).
In addition, the integral compact heat exchanger may offer a large surface area and improved film coeficients help increase the thermal performannce .

Specifically, an integral compact heat exchanger technology was developed and its performance was verified through modeling and experiments. The heat exchanger consists of a reticulated metal foam made out of a high thermal conductivity material such as Al or Cu, and which is metallurgical bonded to the insulating thermal base for maximum performance. The initial configuration of the metal foam has a pore density of 5, 10, 20 and 40 pore per

inch (ppi). It is approximately at 8% theoretical density and made made out of, 1100 Al, C102 Cu or Ag.

The initial macro-structure of the foam is considered isotropic with randomly oriented ligaments orientation. In the micro scale the foam structure consists of cells shaped as 14 sided polygons (tetracaidechadron).

The important parameters of the foam are; thermal conductivity, heat transfer surface area and stiffness. The thermal conductivity of 10 % dense foam is estimated to be approximately 5% of its bulk conductivity. This is because of the increased length of the thermal path, and it is related to the orientation of ligaments. Ligaments need to be oriented in the direction of the conductive heat flux which is perpendicular to the plane of power devices.

The effective surface area of the foam depends on the ligament dimensions and the theoretical density. The manufacturers data (Leyda, 1987) show that the surface area of 10% dense foam is 20, 50 and 80 in^2/in^3 for 10, 20 and 40 ppi foams, respectively. Both the surface area and the thermal conductivity of a give foam can be improved by compressing it in the plane perpendicular to the desired direction of the heat flux. Such a compression increases the thoretical density of the foam and aligns the ligaments in the direction of the heat flux.

The compliance of foam depends on the linear elastic, non-linear elastic and non linear plastic characteristics. The elastic modulus of the foam is controlled by the bending of the ligaments and it is related to the theoretical density of the foam by the

$$\frac{E}{E_s} = C.\left(\frac{\rho}{\rho_s}\right)^2 \qquad (2.1)$$

following relationship (Ashby, 1983) where s refers to the modulus (E) and the density (ρ) properties of the solid material, and C is a know constant the value of which is about 1. The maximum stress on the stress strain curve is bounded by the elastic buckling of the ligaments. Once the elastic collapse takes place, the maximum stress is limited to 5% of the apparent modulus (~500 psi) which further reduces the effective modulus of the material. The foam may also collapse by plastic deformation. When the plastic moment of the cell ligament is exceeded, plastic hinges develop causing large deformations at practically a constant level of stress. The plastic collapse stress of a 10% dense material is about 1% of the yield stress of the solid material (~50 psi for 1100 Al). Both the elastic and the plastic collapse of foam structure reduce the effective modules and limits the maximum stresses that foam can support. Therefore, the reticulated metal foam structure has a very high effective compliance that allows us to hard bond the foam by soldering or brazing to low CTE materials. Since the CTE mismatch related thermal stresses and deformations are limited, the reliability of the integral heat exchanger/thermal base is not comprimised as verified by hundreds of power cycles.

Due to its high thermal conductivity, compatibility with DI water, and solderability to copper metalized surfaces Cu102 based reticulated foam structure was selected for near term studies as the compact heat exchanger material.

The 40 ppi 8 % dense Cu foam material was biaxially compressed to 40% theoretical density and soldered bonded to Cu metalized AlN thermal bases. The top surface of the AlN thermal base was metalized with 0.003" Cu that was patterned to provide isolation for the TP switches. The bottom surface was blanket metalized with 0.003" Cu. To form the integral heat exchanger the Cu foam was bonded by either using CuSil braze alloy or by using 90/10 Pb/Sn high temperature soldering alloy to the bottom surface of the thermal base.

The structure of the as fabricated and compressed foams are shown below.

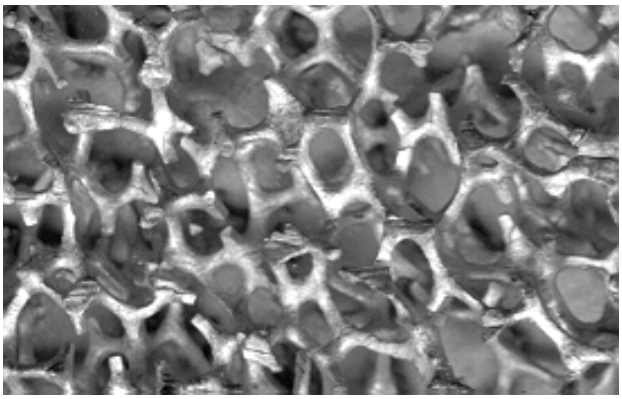

Figure 13. 10 ppi, 8% dense Cu foam. The ligament diameter:~ 0.016", and ligament length: ~ 0.100".

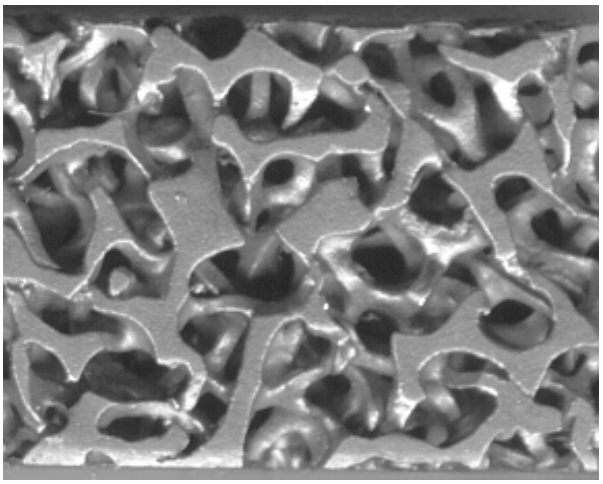

Figure 14. 10 ppi 8% dense foam compressed to 40% density. Direction of compression is perpendicular to the plane.

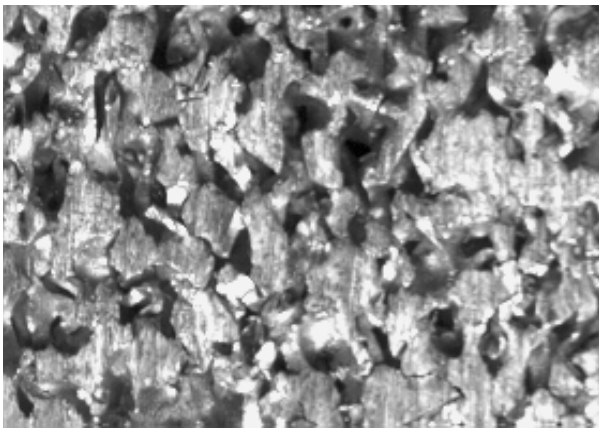

Figure 15. 10 ppi 8% dense Cu foam was laterally compressed to 40% density. Direction of compression is along thelong edge.

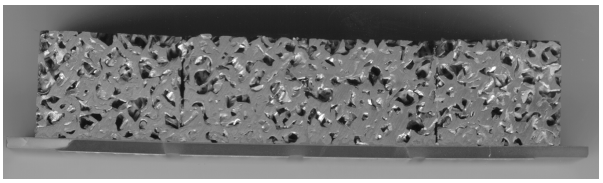

Figure 16. A 40 ppi 40% dense foam with (2.00"x1.3"x0.325") dimensions soldered on an Cu metalized ALN thermal base plate.

The pore and the relative density of foam, the thickness of foam and the coolant are among the key design variables that will strongly influence the maximum thermal performance of foam based heat exchangers.

An analytical model was developed to study the sensitivity of thermal performance limits on the design variables. The model assumes that due to compression of the foam in the x and y directions the z conductivity is dominant. The heat flux from a thermal base of unit area may be obtained from the energy balance and it is given by (2.2). The heat flux was assumed zero at the end of foam.

$$q = k.n.t.w.\theta_b.Tanh(n.L) \qquad (2.2)$$

and

$$n = \sqrt{\frac{\bar{h}_m.\lambda}{k}}$$

$$\lambda = \rho.\ \psi$$

$$k = k_m.\rho.\zeta$$

where;

q : Heat flux at the base (W / in^2 -^{o} C)
k_m: Thermal conductivity of bulk foam material in z direction ($W / m -^{o}$C)
t : Thickness of foam ($Inch$) $= 1$
w : Width of foam ($Inch$) $= 1$
L : Length of foam ($Inch$)
θ_b: (T_b – T) Temperature (^{o}C)
h_m: Maximum film coefficient ($W / in^2 -^{o} C$), $h_m \approx 6.54$ for force convection with water. $h_m \approx 0.0654$ for force convection with air
λ : Heat transfer area per unit volume per unit density (in^2 / in^3)
ρ : Volumetric density of foam
ζ : A geometric factor $\sim 1/3$
ψ: A geometric factor (13.14, 6, 2.43 for 40, 20 and 10 ppi foams

The predictions of the model are show below for 40 ppi foams as a function of the volumetric density and the thickness of foam. The vertical axis shows the value of the heat flux from a unit base area for a unit temperature difference between the base and the coolant. The calculations were made for both water and air. The results show that the effective thickness of foam strongly depend on the film coefficient attainable with a specific coolant.

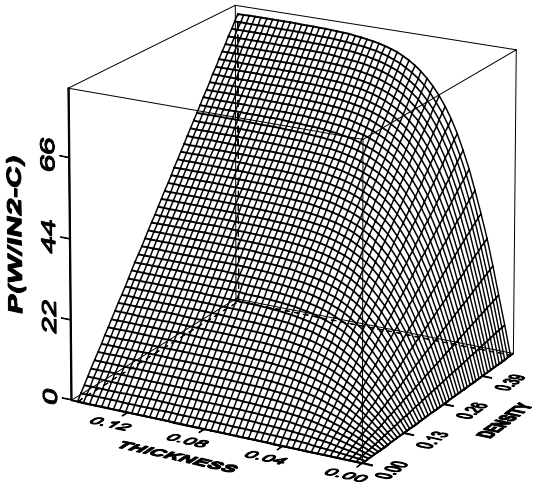

Figure 17. Thermal performance of a water cooled sytem using 40 ppi Cu foam.

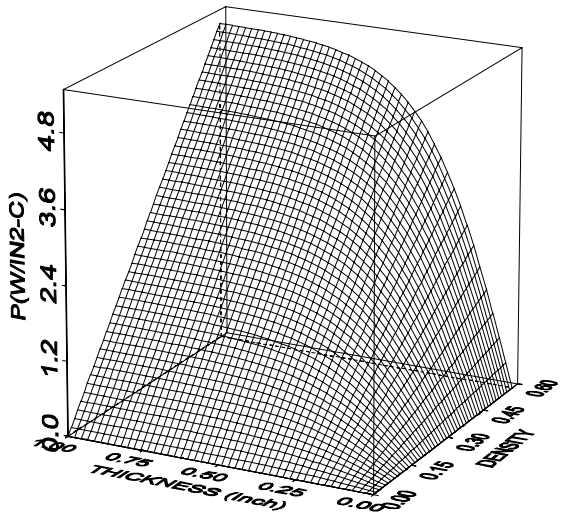

Figure 18. Thermal performance of a air cooled sytem using 40 ppi Cu foam.

Experimentally, to verify the performance of foam based heat exchangers a thermal test module was designed and built. The thermal test module employes (4) size 8 IGBT TP in series as a set of variable resistors. The dissipation of each IGBT TP can be independently varied by changing the gate voltage. The temperature of each IGBT TP was monitored by using thermocouples attached to TPs. During a typical test, the power dissipation in each resistor, temperature of each resistor, flow rate and the flow resistance and the inlet and outlet temperature of the coolant was monitored.

A series of tests were run at 1000 W dissipation level and at varying flow rates. The test module used a 40 ppi 40% dense and biaxially compressed 0.325" thick Cu foam. The results of these tests are shown below.

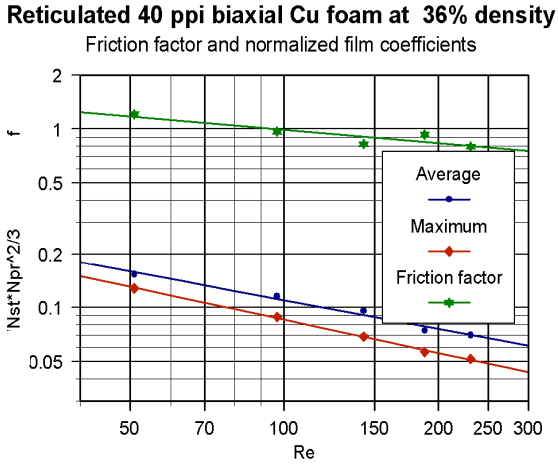

Figure 19. The heat transfer and flow friction data for 40 ppi, 40% dense Cu foam based heat exchangers.

To evaluate the thermal performance of various power module configurations, several 3D FEA and experiments were performed. The effect of materials and dimensions of heat spreaders, external thermal interfaces and spacing of power dies was analyzed. Figures 20 and 21 show the FEM of compact and large foot print power modules

The power modules included the same two-switch configuration where each switch consisted of multiple (4) HTPs two for power dies and two for diodes. The over all dimensions of a single switch is approximately 0.800"x1.00" when die separation is 0.010". It was assumed that the heat was uniformly generated in the top 0.004" thickness of 0.016" thick power devices where the active area of the dies and diodes being approximately 1 cm^2 and 0.5 cm^2, respectively. It was assumed that the heat is removed by forced convection to the coolant water at 0 ^oC temperature. The total dissipation level is 1400W per module, 700 W per switch, 300W per power die and 50W per power diode.

Table 1 shows the thickness and the thermal conductivity of each layer in the module stacks.

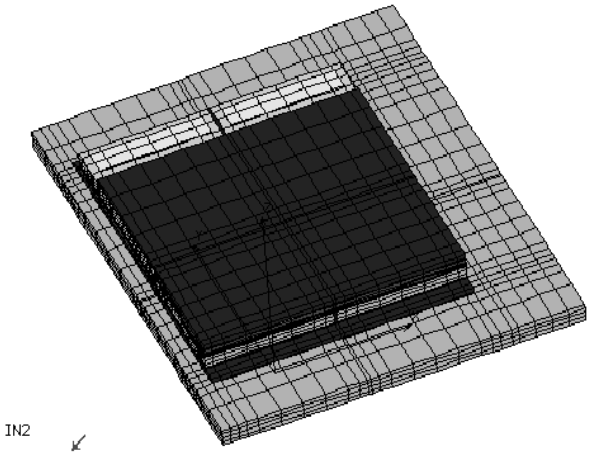

Figure 20. A half symmetry FEM of a compact power module with two switches on ~ 3 in^2 base area.

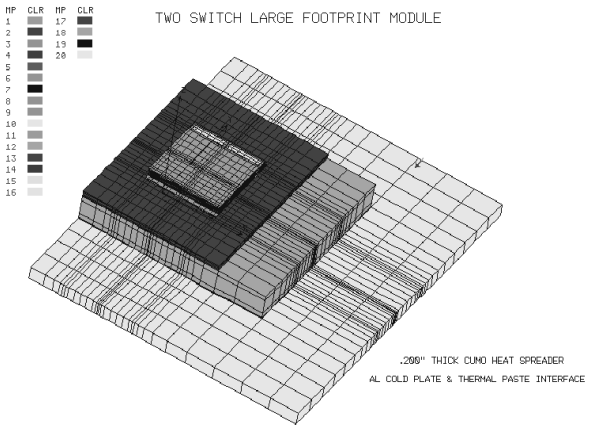

Figure 21. A half symmetry FEM of a compact power module with two switches on a 10 in2 base area.

The effective film coefficients and surface area multiplier factors were used in modeling the convective aspects of the heat transfer. It was assumed that the film coefficient h is 1 $W/^oC/cm^2$ (Mahalingam, 1985), and the effective surface area multipliers are 1 for the baffled heat sink cavity with a flat module base, 2 for a typical commercial cold plate and 6 for the high performance integral compact heat exchanger

	t (inch)	**K_{th} ($W/cm-^oC$)**
Cu electrodes	0.010	3.900
Solser (S1, S2, S4)	0.002	0.040
Solder (S3)	0.002	0.300
Lid metalization (Al)	0.002	1.800
Lid (Al_2O_3)	0.025	0.300
Lid (AlN)	0.025	0.025
Silicon	0.016	0.800
Heat spreader (AlSiC)	0.100	1.700
Heat spreader (CuMo)	0.100	2.700
Thermal paste (effective)	0.004	0.008
External heat sink (Al)	0.100	2.000

Table 1. Thickness and thermal conductivity of the materials in the module stack.

The baffled heat sink consists of an external cavity with baffled flow passages. It is then mechanically coupled to the thermal base of the power module to provide turbulent flow conditions in contact with the flat base. The effective area multiplier factor for the integral heat exchanger was determined by matching the experimental and modeling results to obtain the same maximum junction temperature. The results of the FEA and the experiments for several module configurations are given in the Table 2. It is noted that the test results were obtained using the test midule with 3.2 in2 base area and 4 size 8 devices (Total area of dissipation is approximately 1 in2. The thermal resistance values for the integral foam based heat exchangers (not for the baffled or external heat exchanger cases) need to be scaled with a factor of 0.33 to estimated the performance limit on the test module configuration. This because of the observation that the effect of heat spreading is insignificant for the integral faom based heat exchangers.

The thermal performance of advanced power modules may be improved by a factor of 2 if a high performance integral heat exchanger is incorporated in to the design. The results show that the effect of heat spreaders may be easily shadowed by the method of heat sinking. The CTE mismatch between the insulating thermal bases such as AlN or BeO and the heat spreader material may lead to reliability problems related to low cycle thermal fatigue. Therefore, the heat spreader materials suitable for the advanced dual use high performance

		AREA (IN2)	HEAT SPREADER	HEAT SINK	ΔT_{j-a}, max (^{o}C)	R ja (^{o}C/W)	P max. @ $\Delta T_{ja} = 60\ C$
1	**C**	10.2	AlSiC - 0.100"	EXTERNAL	178	0.127	470
2	**C**	10.2	AlSiC - 0.200"	EXTERNAL	163	0.116	515
3	**C**	10.2	AlSiC - 0.200"	EXTERNAL	150[s]	0.107	560
4	**C**	10.2	CuMo - 0.200"	EXTERNAL	147	0.105	571
5	**C**	10.2	CuMo - 0.200"	EXTERNAL	129 [s]	0.092	651
6	**C**	10.2	CuMo - 0.100"	EXTERNAL	164	0.117	512
7	**C**	10.2	CuMo - 0.100"	BAFFLED CAVITY	121	0.086	694
8	**C**	10.2	CuMo - 0.100"	INTEGRAL	70	0.050	1,200
9	**C**	10.2	Cu - 0.150"	EXTERNAL	137	0.980	613
10	**C**	3.2	NONE	EXTERNAL	264	0.189	318
11	**C**	3.2	NONE	BAFFLED CAVITY	162	0.116	519
12	**C**	3.2	NONE	INTEGRAL	60	0.043	1,400
13	**E**	3.2	NONE	BAFFLED CAVITY	75 ^{o}C @ 800W	0.095	640
14	**E**	3.2	NONE	EXTERNAL	95 ^{o}C @ 800W	0.120	505
15	**E**	3.2	NONE	INTEGRAL-40ppiAl-10%	86 ^{o}C @ 800W	0.108	560
16	**E**	3.2	NONE	INTEGRAL-40ppiAl-20%	69 ^{o}C @ 850W	0.080	740
17	**E**	3.2	NONE	INTEGRAL-40ppiAl-36%	47 ^{o}C @ 850W	0.059	1020
18	**E**	3.2	NONE	INTEGRAL-40ppiCu-40%	38 ^{o}C @ 800W	0.047	1265
19	**E**	3.2	NONE	INTEGRAL-40ppiCu-40%	63 ^{o}C @ 1000W$^{E/G}$	0.063	950
20	**E**	3.2	NONE	INTEGRAL-40ppiCu-40%	35 ^{o}C @ 500W^{EO}	0.070	860

S : die seperation is 0.310 inch otherwise 0.010 inch
E :Experimental, C:Calculated
E/G: 50% Water-Ethylene Gylcol mixture
EO : Motor Oil, Castrol 399.

TABLE 2. Results of 3D FEA of thermal performance for various power module configurations

power modules are the low expansion high thermal conductivity metal-metal or metal-ceramic composites. Although the advantages of heat spreading for thermal performance may not be debated, the low cost, low weight and reduced size requirements for advanced power module may be more readily achieved by integral heat exchangers than heat spreaders.

SUMMARY

A new approach to packaging high performance power devices was presented. It was shown that to take advantage of high switching speeds and current ratings of advanced power devices, which are being developed in response to ever demanding size, weight, performance and cost requirements of commercial and military applications, advanced cost effective packaging approaches will be necessary. The most critical technical challenges facing the advanced packaging technologies are related to the package parasitics and the rates of high heat dissipation.

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